



**QUEEN'S  
UNIVERSITY  
BELFAST**

## **Closed-Form Design Equations for Class-EM Power Amplifier with Isolation Circuit**

Safari Mugisho, M., & Thian, M. (2018). Closed-Form Design Equations for Class-EM Power Amplifier with Isolation Circuit. In *2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC): Proceedings* Institute of Electrical and Electronics Engineers Inc..  
<https://doi.org/10.1109/INMMiC.2018.8430014>

### **Published in:**

2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC): Proceedings

### **Document Version:**

Peer reviewed version

### **Queen's University Belfast - Research Portal:**

[Link to publication record in Queen's University Belfast Research Portal](#)

### **Publisher rights**

© 2018 IEEE.

This work is made available online in accordance with the publisher's policies. Please refer to any applicable terms of use of the publisher.

### **General rights**

Copyright for the publications made accessible via the Queen's University Belfast Research Portal is retained by the author(s) and / or other copyright owners and it is a condition of accessing these publications that users recognise and abide by the legal requirements associated with these rights.

### **Take down policy**

The Research Portal is Queen's institutional repository that provides access to Queen's research output. Every effort has been made to ensure that content in the Research Portal does not infringe any person's rights, or applicable UK laws. If you discover content in the Research Portal that you believe breaches copyright or violates any law, please contact [openaccess@qub.ac.uk](mailto:openaccess@qub.ac.uk).

# Closed-Form Design Equations for Class- $E_M$ Power Amplifier with Isolation Circuit

Moïse Safari Mugisho

Queen's University Belfast, ECIT Institute  
Belfast, Northern Ireland  
m.safari@qub.ac.uk

Mury Thian

Queen's University Belfast, ECIT Institute  
Belfast, Northern Ireland  
m.thian@qub.ac.uk

**Abstract**— The main circuit of the Class- $E_M$  power amplifier fulfils the ZVS/ZVDS/ZCS/ZCDS conditions while the auxiliary circuit thereof fulfils the ZVS condition. Hence, enabling high-efficiency operations at higher operating frequencies while using active devices with slower switching time, resulting in a low-cost high-efficiency power amplifier. This paper presents a new Class- $E_M$  power amplifier configuration that incorporates an isolation circuit between the main and the auxiliary circuit. Explicit design equations for the load network parameters which fulfils the operational conditions of the Class- $E_M$  power amplifier are derived. The analytical results correlate with the ADS simulations results, showing the potential of achieving a theoretical efficiency of 100% at higher frequencies while using low-cost, slow switching active devices.

**Keywords**—Class- $E_M$ , high-efficiency, isolation circuit, slow-switching, switching amplifier, ZCS, ZCDS, ZVS, ZVDS.

## I. INTRODUCTION

The Class-E power amplifier (PA), introduced in [1], delivers a theoretical efficiency of 100% through adoption of zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions. However, the absence of zero current switching (ZCS) and zero current derivative switching (ZCDS) produces an overlap between a non-zero current and a non-zero voltage across the switch during ON-to-OFF transition, resulting in a power loss that limits the practical efficiency of the Class-E PA. To address this problem, the Class- $E_M$  PA was proposed in [2]. It consists of a main circuit operating at the fundamental frequency ( $f_0$ ) and an auxiliary circuit operating at the second harmonic frequency ( $2f_0$ ) as shown in Fig. 4 of [2].

However, the Class- $E_M$  PA has not found widespread usage due to the complexity of the analysis presented thus far and the lack of accurate explicit design equations required to determine the optimum load network parameters. In [2], the main circuit was analysed separately from the auxiliary circuit, resulting in explicit design equations for the main circuit alone but not the auxiliary circuit. In addition, some of the design equations provided in Table I of [2] are incorrect and ambiguous. For example, the provided equation of the load reactance ( $X_L$ ) implies that it is capacitive, but not inductive as indicated in Table I and in the circuit schematic of Fig.4 in [2]. Further, the provided equation for the injection resistance ( $R_{inj}$ ) implies the presence of a physical resistor between the main and the

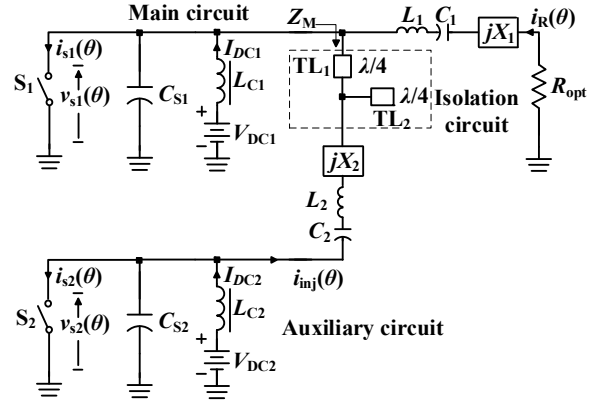


Fig. 1. Class- $E_M$  PA with the proposed transmission-line isolation circuit.

auxiliary circuit, but on the other hand, the model of the Class- $E_M$  PA does not account for such physical resistor. Crucially, the analysis of the auxiliary circuit was not presented in [2], thus, the ZVS condition was not fulfilled in the auxiliary circuit, resulting in a poor efficiency of 58% for the auxiliary circuit although the main circuit exhibits a high efficiency of 89%. This issue was addressed in [3]-[4] where both the main and auxiliary circuits were analyzed simultaneously, but this results in a large system of nonlinear equations requiring to be solved by numerical methods, thus adding to the complexity in the design of a Class- $E_M$  PA. Furthermore, we failed to reproduce the idealized switch voltage and current waveforms using the component values provided in Table IV of [4].

The simultaneous analysis presented in [5]-[6], takes into account the interaction between the main and the auxiliary circuit at  $f_0$ ,  $2f_0$  and  $3f_0$  resulting in a large system of equations with no explicit design equations provided. The claim in [6], that “to obtain the optimum load network parameters of the Class- $E_M$  PA, it is necessary to take into account up to the third harmonic components of the injected current and the load current” will be refuted in this paper.

In this paper it will be shown that, the analysis of the Class- $E_M$  PA can be simplified and accurate explicit design equations for the load network parameters can be derived. This is made possible by incorporating an isolation circuit between the main and the auxiliary circuit, resulting in a new configuration of the Class- $E_M$  PA as depicted in Fig. 1. Consequently, the analysis of the main and auxiliary circuits can be performed separately,

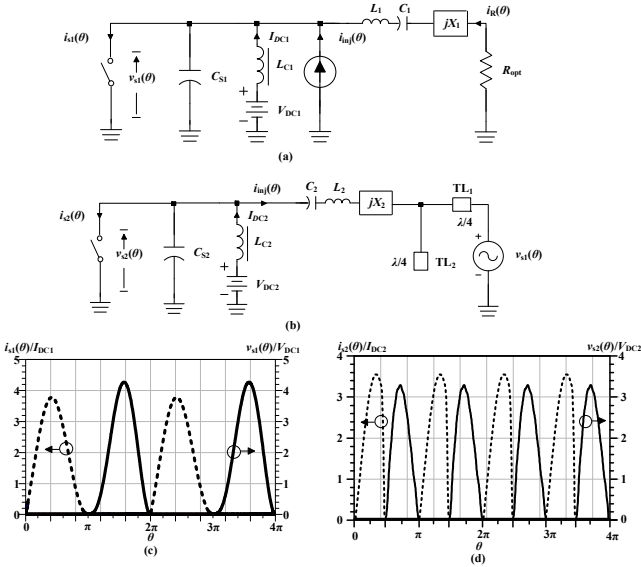


Fig. 2. (a) Class-E<sub>M</sub> PA with the auxiliary circuit modelled as a current source, (b) Class-E<sub>M</sub> PA with the main circuit modelled as a voltage source, (c) idealized main switch voltage and current waveforms, (d) idealized auxiliary switch voltage and current waveforms.

thus, reducing the complexity of the analysis while obtaining accurate and explicit design equations. Moreover, the operational relationship between the main and the auxiliary circuit is clearly derived and the contribution of each circuit to the overall performance of the Class-E<sub>M</sub> PA will be explained through our analysis. It will be shown that the load network parameters of the auxiliary circuit can be directly obtained from the load network parameters of the main circuit, thus, establishing an unambiguous design procedure for the Class-E<sub>M</sub> PA. An idealized Class-E<sub>M</sub> PA is designed and simulated to verify the accuracy of the design equations derived from the analysis presented in this paper.

This paper is organised as follows: the idealized circuit operation of a Class-E<sub>M</sub> PA is discussed in Section II. Section III presents the circuit analysis of a Class-E<sub>M</sub> PA. Finally, the design of a Class-E<sub>M</sub> PA is presented in Section IV.

## II. IDEALIZED CIRCUIT OPERATION

The new configuration of the Class-E<sub>M</sub> PA as shown in Fig. 1, consists of a main circuit, an auxiliary circuit and the newly introduced isolation circuit. The main and the auxiliary circuits consist of a shunt capacitance ( $C_{s1}$  and  $C_{s2}$ ), a series resonant circuit ( $L_1C_1$  tuned at  $f_0$  for the main circuit and  $L_2C_2$  tuned at  $2f_0$  for the auxiliary circuit), a series reactance ( $X_1$  and  $X_2$ ), and an RF choke ( $L_{C1}$  and  $L_{C2}$ ).

The purpose of the auxiliary circuit is to inject a second harmonic current with a specific amplitude and phase into the switch of the main circuit, while still fulfilling the ZVS condition of a classical Class-E PA. The injected second harmonic current allows the main circuit to fulfil the ZVS/ZVDS/ZCS/ZCDS conditions, resulting in soft switching during ON-to-OFF and OFF-to-ON transitions, which in turn minimizes the power loss in the switch and maximizes the efficiency of the PA.

The isolation circuit consists of a series  $\lambda/4$  transmission line (TL<sub>1</sub>) and an open-circuited  $\lambda/4$  stub (TL<sub>2</sub>), which enforces a short-circuit termination at  $f_0$  and  $(2n+1)f_0$ . This short-circuit termination is transformed into an open-circuit termination by TL<sub>1</sub>. Thus, the impedance presented by the auxiliary circuit to the main circuit ( $Z_M$ ) is sufficiently high, isolating the main circuit from the auxiliary circuit at  $f_0$  and  $(2n+1)f_0$ . At  $2nf_0$ , TL<sub>2</sub> enforces an open-circuit termination, thus allowing the injected second-harmonic current to flow through TL<sub>1</sub>.

## III. CIRCUIT ANALYSIS

In order to simplify the analysis of the Class-E<sub>M</sub> PA shown in Fig. 1, the assumptions made in [1] are applied here. Since the main and auxiliary circuits are isolated at  $f_0$  and  $3f_0$  while interacting at  $2f_0$ , the isolation circuit and auxiliary circuit from Fig. 1 can be replaced with an ideal current source, resulting in the circuit depicted in Fig. 2a. The optimum Class-E<sub>M</sub> switching conditions are given in (1)-(3).

$$v_{s1}(\theta)|_{\theta=2\pi} = 0 \quad \text{and} \quad \left. \frac{dv_{s1}(\theta)}{d\theta} \right|_{\theta=2\pi} = 0 \quad (1)$$

$$i_{s1}(\theta)|_{\theta=\pi} = 0 \quad \text{and} \quad \left. \frac{di_{s1}(\theta)}{d\theta} \right|_{\theta=\pi} = 0 \quad (2)$$

$$v_{s2}(\theta)|_{\theta=\pi} = 0 \quad (3)$$

The load current  $i_R(\theta)$  and injected current  $i_{inj}(\theta)$  are given by (4), where  $\theta = \omega t$  (rad),  $I_R$  is the amplitude of the load current,  $\alpha$  is the initial phase shift at  $f_0$ ,  $I_{inj}$  is the amplitude of the injected current, and  $\beta$  is the phase shift of the injected current at  $2f_0$ .

$$i_R(\theta) = I_R \sin(\theta + \alpha) \quad \text{and} \quad i_{inj}(\theta) = I_{inj} \sin(2\theta + \beta) \quad (4)$$

When the main switch  $S_1$  is turned ON for a period of  $0 \leq \theta \leq \pi$ , the current  $i_{s1}(\theta)$  flowing through  $S_1$  is given by (5) while the voltage  $v_{s1}(\theta)$  across  $S_1$  is zero.

$$i_{s1}(\theta) = I_{DC1} + i_{inj}(\theta) + i_R(\theta) \quad (5)$$

When  $S_1$  is turned OFF for a period of  $\pi \leq \theta \leq 2\pi$ ,  $i_{s1}(\theta)$  flows through  $C_{s1}$  and  $v_{s1}(\theta)$  is given by (6).

$$v_{s1}(\theta) = \frac{1}{\omega C_{s1}} \int_{\pi}^{\theta} i_{s1}(\theta) d\theta \quad (6)$$

Applying the switching conditions in (1)-(2) and the initial OFF condition to (5) and (6) results in a set of equations with unknown parameters  $I_R$ ,  $\alpha$ ,  $I_{inj}$ , and  $\beta$ . The solutions to these equations provide the first set of design equations (7)-(8).

$$I_R = \frac{\pi}{2} I_{DC1} \quad \text{and} \quad \alpha = 0^\circ \quad (7)$$

$$I_{inj} = -\frac{\sqrt{\pi^2 + 16}}{4} I_{DC1} \quad \text{and} \quad \tan(\beta) = -\frac{4}{\pi} \quad (8)$$

The average value of  $v_{s1}(\theta)$  in (6) is the DC voltage  $V_{DC1}$ , from which the design equation for  $C_{s1}$  can be obtained as in (9).

$$C_{s1} = \frac{\pi I_{DC1}}{16 \omega V_{DC1}} \quad (9)$$

Using (7) and Fourier series expansion for  $v_{s1}(\theta)$ , the load resistance ( $R_{opt}$ ) and the load reactance ( $X_1$ ) can be obtained as follows.

$$R_{opt} = \frac{32 V_{DC1}}{3\pi^2 I_{DC1}} \quad \text{and} \quad X_1 = \frac{8(3\pi^2 - 32) V_{DC1}}{3\pi^3 I_{DC1}} \quad (10)$$

The total output power  $P_{out}$  of the Class-E<sub>M</sub> PA given in (11) and derived from (7) and (10), shows that  $P_{out}$  is four third of the DC power of the main circuit

$$P_{out} = \frac{4 V_{DC1} I_{DC1}}{3} = \frac{4}{3} P_{DC1} \quad (11)$$

The normalized main switch waveforms depicted in Fig. 2c shows that the ZVS/ZVDS/ZCS/ZCDS conditions are met, and that the peak main switch current and voltage are  $3.77 \times I_{DC1}$  and  $4.27 \times V_{DC1}$ , respectively, and this can be proven from (5) and (6).

To simplify the analysis of the auxiliary circuit, the main circuit is replaced by an equivalent voltage source  $v_{s1}(\theta)$ , resulting in the circuit depicted in Fig. 2b. When the auxiliary switch  $S_2$  is turned ON for a period of  $0 \leq \theta \leq \pi/2$ , the current  $i_{s2}(\theta)$  flowing through  $S_2$  is given by (12) while the voltage  $v_{s2}(\theta)$  across  $S_2$  is zero.

$$i_{s2}(\theta) = I_{DC2} - i_{inj}(\theta) \quad (12)$$

When  $S_2$  is turned OFF for a period of  $\pi/2 \leq \theta \leq \pi$ ,  $i_{s2}(\theta)$  flows through  $C_{s2}$  and  $v_{s2}(\theta)$  is given by (13).

$$v_{s2}(\theta) = \frac{1}{\omega C_{s2}} \int_{\pi/2}^{\theta} i_{s2}(\theta) d\theta \quad (13)$$

Applying the switching conditions in (3) to (13) results in a single equation, the solution of which provides the design equation for  $I_{DC2}$  given in (14), from which it can be seen that the DC current of the auxiliary circuit is half that of the main circuit.

$$I_{DC2} = \frac{I_{DC1}}{2} \quad (14)$$

The average value of  $v_{s2}(\theta)$  in (13) is the DC voltage  $V_{DC2}$ , from which the design equation for  $C_{s2}$  can be obtained as in (15).

$$C_{s2} = \frac{I_{DC2}}{\pi \omega V_{DC2}} \quad (15)$$

Using Fourier series expansion for  $v_{s1}(\theta)$  and  $v_{s2}(\theta)$  and applying KVL to the circuit of Fig. 2b, it can be shown that the in-phase components of  $v_{s1}(\theta)$  and  $v_{s2}(\theta)$  adds to zero, thus justifying the absence of any physical resistor between the main and the auxiliary circuit. Furthermore, the sum of the quadrature components of  $v_{s1}(\theta)$  and  $v_{s2}(\theta)$  provides the amplitude of the voltage across the reactance  $X_2$ , which together with (8) are used to determine  $X_2$ .

$$X_2 = \frac{(\pi^2 + 4) V_{DC2}}{8 \pi I_{DC2}} \quad (16)$$

Using (11) and (14), it can be shown that the DC power of the auxiliary circuit  $P_{DC2}$  is one third of  $P_{DC1}$ , consequently,  $V_{DC2}$  is two third of  $V_{DC1}$ , thus establishing a clear operational relationship between the main and the auxiliary circuit, such that the design equations of the auxiliary circuit can be determined from those of the main circuit. The normalized auxiliary switch waveforms depicted in Fig. 2d shows that the auxiliary circuit fulfils the ZVS condition and that the peak auxiliary switch current and voltage are  $3.55 \times I_{DC2}$  and  $3.29 \times V_{DC2}$ , respectively, and this can be proven from (12) and (13).

#### IV. DESIGN AND VERIFICATION

To verify the accuracy of the design equations derived in Section III, a high-efficiency Class-EM PA was designed and simulated in ADS. The specifications were set as  $V_{DC1} = 28$  V,  $I_{DC1} = 0.5$  A and  $f_0 = 2.2$  GHz, resulting in  $I_{DC2} = 0.25$  A,  $V_{DC2} = 18.667$  V,  $P_{DC1} = 14$  W, and  $P_{DC2} = 4.666$  W. The load

network parameters of the main circuit were determined as  $C_{s1} = 0.253$  pF,  $R_{opt} = 60.52$  Ohm, and  $C_{x1} = 6.282$  pF using (9)-(10). The load network parameters of the auxiliary circuit were determined as  $C_{s2} = 0.308$  pF and  $L_{x2} = 2.98$  nH using (15)-(16). The characteristic impedances of the isolation circuit were selected as 50 Ohm. A  $P_{out}$  of 42.71 dBm (18.662 W) was simulated as shown in Fig. 3 thus confirming the design equation in (11) and resulting in 99.97% efficiency. A peak main switch current and voltage of  $3.777 \times I_{DC1}$  and  $4.273 \times V_{DC1}$  respectively and a peak auxiliary switch current and voltage of  $3.551 \times I_{DC2}$  and  $3.291 \times V_{DC2}$  were simulated confirming the analytical predictions.

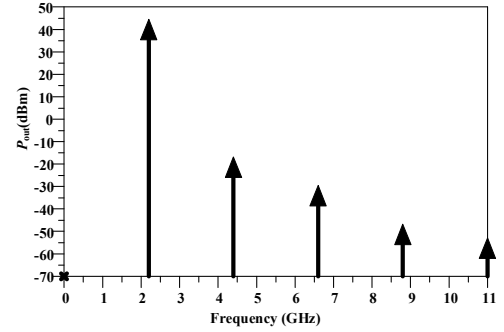


Fig. 3. Simulated output power spectrum of the proposed Class-EM PA.

#### V. CONCLUSION

The analysis of a new Class-EM PA configuration resulting in explicit design equations and an unambiguous design procedure has been presented. The accuracy of the presented analysis was verified with the design and simulation of an idealized Class-EM PA that fulfils the ZVS/ZVDS/ZCS/ZCDS conditions on the main circuit as well as the ZVS condition on the auxiliary circuit. Thus, showing the possibility of achieving high-efficiency at higher operating frequencies with low-cost slow switching devices. The proposed isolation circuit constitutes a first step towards the first implementation of a high frequency transmission lines Class-EM PA.

#### ACKNOWLEDGMENT

This work was supported by the UK EPSRC under grant no. EP/P013031/1.

#### REFERENCES

- [1] N.O. Sokal and A.D. Sokal, "Class-E a new class of high-efficiency tuned single ended switching power amplifiers," *IEEE J Solid-State Circuits*, vol. SC-10, no. 3, pp. 168-176, Jun. 1975.
- [2] A. Telegdy, B. Molnar, and N.O. Sokal, "Class-EM switching-mode tuned power amplifier- high efficiency with slow-switching transistor," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 6, pp. 1662-1676, Jun. 2003.
- [3] R. Miyahara, H. Sekiya, and M.K. Kazimierzczuk, "Design of Class-EM power amplifier taking into account auxiliary circuit," *IECON*, pp. 679-684, 2008.
- [4] R. Miyahara, H. Sekiya, and M.K. Kazimierzczuk, "Novel design procedure for Class-EM power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3607-3615, Dec. 2010.
- [5] Z. Zhang, et al., "Analysis of Class-EM amplifier with considering non-zero current fall time of drain current," *IFEEC*, pp. 338-343, 2013.
- [6] X. Wei, T. Nagashima, M.K. Kazimierzczuk, H. Sekiya, and T. Suetsugu, "Analysis and design of Class-EM power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, pp. 976-986, Apr. 2014.